CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of forming a metal silicate layer in a semiconductor structure comprising the steps of:

(a) forming a metal oxide layer on a silicon-containing material; and

(b) heating said metal oxide layer in the presence of an oxidizing agent under conditions so as to convert the metal oxide layer into a metal silicate layer while simultaneously oxidizing a portion of the silicon-containing material underlying the metal silicate layer.

2. The method of Claim 1, wherein said metal oxide comprises oxygen and at least one metal selected from the group consisting of La, Hf, Y, Sc, Sr, Ba, Ti, Ta, W, Cr, Ca, Mg, Be, Pr, Nd and mixtures and alloys thereof.

3. The method of Claim 2, wherein the at least one metal is La, Hf or Y.

4. The method of Claim 1, wherein said metal oxide is La_2O_3.

5. The method of Claim 1, wherein an elemental metal layer is formed in place of the metal oxide layer

and step (b) converts said metal layer to a metal oxide layer and then to a metal silicate.

6. The method of Claim 1, wherein said silicon-containing material is a Si-containing semiconductor substrate, a silicon-on-insulator, sapphire, SiO_2, SiGe, Si oxynitride or any combination thereof.

7. The method of Claim 1, wherein said silicon-containing material comprises a Si-containing semiconductor substrate having an exposed SiO_2 surface layer.

8. The method of Claim 7, wherein said exposed SiO_2 surface layer is removed prior to conducting step (a).

9. The method of Claim 1, wherein said silicon-contained material is a layered material.

10. The method of Claim 1, wherein said metal oxide layer is formed by a deposition process selected from the group consisting of chemical vapor deposition, plasma-vapor deposition, sputtering, evaporation, reactive deposition and other like deposition processes.

11. The method of Claim 1, wherein said metal oxide layer has a thickness of from about 1 to about 50 Å.

12. The method of Claim 1, wherein step (b) is conducted at a temperature of less than about 950°C for a time period of at least about 10 seconds.

13. The method of Claim 12, wherein step (b) is conducted at a temperature of from about 750° to about 900°C for a time period of from about 60 to about 180 seconds.

14. The method of Claim 1, wherein said oxidizing agent comprises O_2, N_2O or NO.

15. The method of Claim 1 further comprising annealing the metal silicate layer formed in step (b).

16. The method of Claim 15, wherein said annealing is carried out using a forming gas anneal.

17. The method of Claim 16, wherein said forming gas anneal is carried out at a temperature of less than about 700°C for a time period of greater than 1 second.

18. The method of Claim 17, wherein said forming gas anneal is carried out at a temperature of from about 350°C to about 650°C for a time period of from about 10 seconds to about 1 hour.

19. The method of Claim 1 further comprising forming an electrically conductive contact on the surface of said metal silicate.

20. The method of Claim 19, wherein said electrically conductive contact is polysilicon, W, Al or Pt.

21. A semiconductor structure comprising at least a metal silicate that is formed on a silicon oxide layer, said silicon oxide layer being formed on a Si-containing semiconductor substrate.

22. The semiconductor structure of Claim 21, wherein said metal silicate comprises at least a metal selected from the group consisting of La, Hf, Y, Sc, Sr, Ba, Ti, Ta, W, Cr, Ca, Mg, Be, Pr, Nd and mixtures and alloys thereof.

23. The semiconductor structure of Claim 22, wherein said metal is La, Hf or Y.

24. The semiconductor structure of Claim 21, wherein said metal silicate is a La silicate.

25. The semiconductor structure of Claim 21, wherein said silicon oxide layer has a thickness of from about 5 to about 10 Å.

26. The semiconductor structure of Claim 21, wherein said metal silicate has a thickness of from about 20 to about 50 Å.

27. The semiconductor structure of Claim 21, wherein said structure has a leakage current below 1×10^{-4} amps/cm^2 at -1 volts and a capacitance density of greater than 5×10^{-6} F/cm^2.

28. A field effect transistor comprising:

a Si-containing semiconductor substrate;

spaced apart source/drain regions in said substrate defining a channel region therein;

a dielectric layer above said channel region, said dielectric layer including a first layer of a metal silicate; and

a gate electrode formed over said dielectric layer.

29. The field effect transistor of Claim 28, wherein said metal silicate comprises at least a metal selected from the group consisting of La, Hf, Y, Sc, Sr, Ba, Ti, Ta, W, Cr, Ca, Mg, Be, Pr, Nd and mixtures and alloys thereof.

30. The field effect transistor of Claim 29, wherein said metal is La, Hf or Y.

31. The field effect transistor of Claim 28, wherein said silicate is La silicate.

32. The field effect transistor of Claim 28, wherein said dielectric layer includes a layer of SiO_2 between said substrate and said layer of metal silicate.

33. The field effect transistor of Claim 28, wherein said gate electrode comprises polysilicon, W, Al or Pt.

34. A capacitor comprising at least the metal silicate obtained by Claim 1 sandwiched between the same or different electrode materials.